

SYMBOL SERIAL PERIPHERAL INVOICE & CLEMENT IDENT.			
TERM.	LOC	TERM.	LOC
8000	1	004	289
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8030	1	007	28A
8040	1	309	276
8050	1	300	285
8060	1	107	285
8070	1	008	285
8080	1	018	283
8090	1	005	283
9100	1	201	282
9110	1	008	282
9120	1	003	281
9130	1	103	281
9140	1	102	281
9150	1	002	280
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9170	1	108	28A
9180	1	106	28A
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2460	1	000	019
2470	1	000	019
2480	1	000	019
2490	1	000	019
2500	1	000	019
2510	1	000	019

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IN

NOTES

1. 1 GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE IN VOLTS

- ### 3 BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

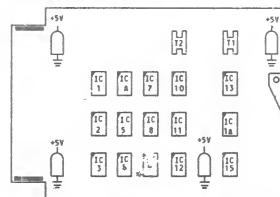
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- 4 BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000.119
GRO	200.319

5. HORIZONTAL MOUNTING CENTERS
AT 0.5 INCH.

6. INTEGRATED CIRCUIT AND TRANSFORMER LOCATION GUIDE
-
- (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION	
CATEGORY	NO.
CIRCUIT PACK CODE	JX5
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE)	1
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELLSYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

JES CIRCUIT PAGE

SERIAL PERIPHERAL INTERFACE A
CIRCUIT

AT&TCO
STANDARD

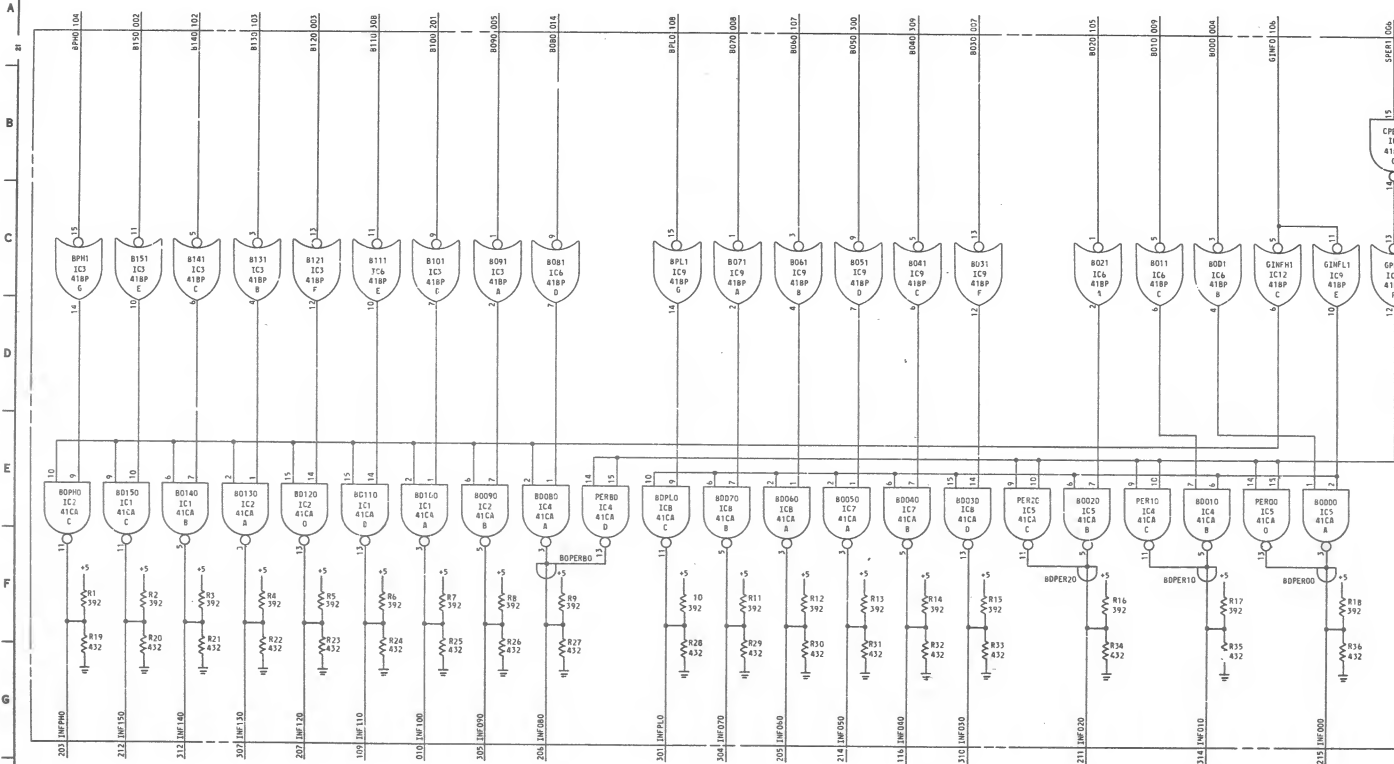
CPS-JK5
A SHEETS

②

BELL TELEPHONE LABORATORIES

66

SERIAL PERIPHERAL INTERFACE A



SERIAL PERIPHERAL INTERFACE A



PART OF CPS JK5

SERIAL PERIPHERAL INTERFACE A

COMPONENT LIST INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 41CA	IC2 41CA	IC3 41BP	IC4 41CA	IC5 41CA	IC6 41BP	IC7 41CA	IC8 41CA	IC9 41BP	IC10 41CA	IC11 41CC
	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC
A	80100 2E2	81130 2C1	80911 2C2	80080 2E3	80000 2E9	8021 2C7	80050 2E5	80040 2E5	8041 2C5	80201 3F2	814 3E4
B	80140 2E1	80990 2E3	8131 2C1	80010 2E8	80020 2E7	8001 2C8	80040 2E4	8041 2C5	8041 2C5	814 3E4	814 3E4
C	80150 2E0	80990 2E0	8141 2C1	8101 2C2	8101 2C2	8041 2C8	8041 2C8	8041 2C8	8041 2C8	814 3E4	814 3E4
D	80110 2E2	80130 2C1	8101 2C2	8101 2C2	8101 2C2	8041 2C8	8041 2C8	8041 2C8	8041 2C8	814 3E4	814 3E4
E			8151 2C0			8111 2C2					
F			8121 2C1			8121 2C1					
G			8101 2C0			8101 2C0					

LOC CODE ELEM ID	IC12 41BP	IC13 41CC	IC14 41CC	IC15 41CC
	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC
A	PT800A 3E1	MP2	3C2	PP3
B	INTP81 304			3C3
C	8101 2C8			8101 2C8
D	8500 3E2			
E	8501 302			
F	8501 300			
G	8501 301			

CAPACITOR

LOC CODE ELEM ID	CODE
C1-C3	25-100PF 15,100PF
C4	600A 1
C5-C8	501A 5
C9-C23	KS-1977A L5,0,1

DIODE

LOC CODE ELEM ID	CODE
CR1,CR2	458C

RESISTOR

LOC CODE ELEM ID	CODE
R1-R18	KS-20616 L14,392
R19-R36	.432
R37	.1000
R38-R40	.432
R41	.301
R42	.365
R43	.182
R44	.243
R45	.301
R46	KS-20616 L14,365

TRANSFORMER

LOC CODE ELEM ID	CODE
(2) T*,T2	26640

CIRCUIT DESCRIPTION:

THIS CIRCUIT PACK CONTAINS 10 BUFFER RECEIVERS AND 10 OPEN COLLECTOR BUS DRIVERS FOR THE 10 INFORMATION LEADS. TRANSMISSION LINE TERMINATIONS ARE PROVIDED BY RESISTIVE VOLTAGE DIVIDERS FOR EACH OF THE INFORMATION LEADS. LEAD 0/MPD BEING LOW GATES THE BUS DRIVERS ON.

LEAD SPEN1 BEING HIGH GATES LEADS INFO00, INFO01, INFO02, AND INFO03 TO GROUND LEVEL. THIS BIT CONFIGURATION IS THE PARITY ERROR REPLY MESSAGE.

THE 50% DUTY CYCLE PULSE TRAIN ON LEAD RSH00A DRIVES THE RETRIGGERABLE MONOPULSER MP1. THE LEADING EDGE OF THE FIRST PULSE SETS THE "1" OUTPUT OF MP1 HIGH. WHEN THE TRIGGERING PULSE TRAIN IS INTERRUPTED BY ABOUT 350 NSEC THE OUTPUT OF MP1 RETURNS TO GROUND LEVEL. THIS GROUND GOING TRANSITION TRIGGERS MP2 TO GENERATE A 350 NSEC WIDE RESET PULSE ON LEAD RSET1 AND RSET01.

THE CABLE DRIVERS CAN BE USED TO TRANSMIT DEMAND INTERRUPT PULSES TO BOTH CCS. THESE PULSES ARE GENERATED BY HIGH TO LOW TRANSITIONS ON LEAD INFO0.

THE RC NETWORK (R37,C4) AT THE INPUT OF SCHMITT TRIGGER ST01 CREATES AN EXPONENTIAL VOLTAGE RISE AS THE +5V POWER IS APPLIED TO THE CIRCUIT. AS LONG AS THE CAPACITOR VOLTAGE IS BELOW THE INPUT THRESHOLD LEVEL OF ST01, THE OUTPUT OF ST01 IS HIGH. THIS HIGH LEVEL KEEPS THE RSET01 LINE ACTIVE. THE SPI CONTROL LOGIC IS INITIALIZED BY THIS HIGH LEVEL.